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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,051	06/27/2003	Kevin W. Glass	80107.022US1	7915

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LeMoine Patent Services  
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EXAMINER
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NGUYEN, LINH M

ART UNIT	PAPER NUMBER
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2816

DATE MAILED: 04/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/608,051	<b>Applicant(s)</b> GLASS, KEVIN W.	
	<b>Examiner</b> Linh M. Nguyen	<b>Art Unit</b> 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 27 June 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-29 is/are pending in the application.  
     4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 12-16 and 26-29 is/are allowed.
- 6) ☒ Claim(s) 1,2,6,7,17-19 and 23-25 is/are rejected.
- 7) ☒ Claim(s) 3-5,8-11 and 20-22 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
     a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>082603</u> . | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

Claims 1-29 are presented in the instant application according to the Applicant's filing on 06/27/2003.

#### *Abstract*

1. The amended abstract of the disclosure is objected to because of its length. Correction is required. See MPEP § 608.01(b).
2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 250 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "**means**" and "**said**," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Correction is required.

#### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Welty et al. (U.S. Patent No. 4,646,103).

With respect to claim 1, Welty et al. discloses, in Figures 1-3, a frequency prescaler comprising a) a first sequential element [10'] having an input stage with at least one embedded

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logic gate [Fig. 1]; and b) a second sequential element [10''] having a clock input node coupled to an output node of the first sequential element.

With respect to claim 2, Welty et al. discloses, in Figures 1-3, that the first sequential element is coupled to perform a conditional divide-by-two operation [Fig. 2, col. 4, lines 37-39].

With respect to claim 6, Welty et al. discloses, in Figures 1-3, that the first sequential element comprises a true single phase clock flip-flop.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Welty et al. (U.S. Patent No. 4, 648, 103) in view of Numata et al. (U.S. Patent No. 4,777,655).

With respect to claim 7, Welty et al. discloses all of the claimed limitations as expressly recited in claim 1, including a) the first sequential element includes a clock input node and b) the first and second sequential elements are configured to form an asynchronous counter. Welty lacks showing that the prescaler receives a voltage controlled oscillator [VCO] output signal.

Numata et al. discloses, in Fig. 2, a prescaler [11] receiving an output from VCO [13] as part of a phase locked loop (PLL) synthesizer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to configure the prescaler for receiving an output from a VCO as taught by Numata to provide a divided output for the process of synchronization in a PLL synthesizer since such a circuit

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arrangement of the prescaler and the VCO for the stated purpose has been a well known practice as evidenced by the teachings of Numata et al.

7. Claims 17-19 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Numata et al. (U.S. Patent No. 4,777,655) in view of Welty et al. (U.S. Patent No. 4,648,103).

With respect to claims 17-19, Numata et al. discloses in Fig. 2, a frequency synthesizer including a) a comparison circuit [12] to compare a reference signal [22] and a frequency divided signal [10]; b) a voltage controlled oscillator [13] to synthesize an output signal in response to the comparison circuit; and a prescaler [11] coupled to the voltage controlled oscillator to divide a frequency of the output signal.

Numata lacks disclosing the details of the prescaler including an asynchronous divider with at least one true single phase clock flip-flop having embedded logic in an input stage; wherein i) the at least one true single phase clock flip-flop includes a least significant flip-flop coupled to be clocked by the output signal, the least significant flip-flop including an input stage having an embedded logic gate and ii) wherein the at least one true single phase clock flip-flop further includes a more significant flip-flop coupled to be clocked by a signal produced by the least significant flip-flop.

Welty et al. discloses, in Figs. 1-3, details of a prescaler including an asynchronous divider with at least one true single phase clock flip-flop having embedded logic [Fig. 1] in an input stage; wherein i) the at least one true single phase clock flip-flop includes a least significant flip-flop [10'] coupled to be clocked by the output signal [C], the least significant flip-flop including an input stage having an embedded logic gate [Fig. 1] and ii) wherein the at least one

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true single phase clock flip-flop further includes a more significant flip-flop [10''] coupled to be clocked by a signal produced by the least significant flip-flop.

To configure the frequency prescaler of Numata et al. with a frequency prescaler which includes all the listed above limitation/details, as taught by Welty et al., that is suitable for fabrication in integrated circuit form in which the divide ratio thereof can be altered after fabrication would have been obvious to one of ordinary skill in the art at the time of the invention since Welty et al. teaches that such a configuration would satisfy the desire of altering the divide ratio without altering the number of flip-flop circuits used (*see Welty et al., col. 1, lines 56-58 and col. 2, lines 1-4*).

8. With respect to claims 23-25, Numata et al. discloses in Figs. 1 and 2, an electronic system that includes 1) a direct conversion receiver [3] with an oscillator input port, 2) a directional antenna [2] coupled to the direct conversion receiver, and 3) a frequency synthesizer coupled to the oscillator input port, the frequency synthesizer comprising a) a comparison circuit [12] to compare a reference signal and a frequency divided signal; b) a voltage controlled oscillator [13] to synthesize an output signal in response to the comparison circuit; and c) a prescaler [11] coupled to the voltage controlled oscillator to divide a frequency of the output signal.

Numata lacks disclosing the details of the prescaler including an asynchronous divider with at least one true single phase clock flip-flop having embedded logic in an input stage; wherein i) the at least one true single phase clock flip-flop includes a least significant flip-flop coupled to be clocked by the output signal, the least significant flip-flop including an input stage

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having an embedded logic gate and ii) wherein the at least one true single phase clock flip-flop further includes a more significant flip-flop coupled to be clocked by a signal produced by the least significant flip-flop.

Welty et al. discloses, in Figs. 1-3, details of a prescaler including an asynchronous divider with at least one true single phase clock flip-flop having embedded logic [Fig. 1] in an input stage; wherein i) the at least one true single phase clock flip-flop includes a least significant flip-flop [10'] coupled to be clocked by the output signal [C], the least significant flip-flop including an input stage having an embedded logic gate [Fig. 1] and ii) wherein the at least one true single phase clock flip-flop further includes a more significant flip-flop [10''] coupled to be clocked by a signal produced by the least significant flip-flop.

To configure the frequency prescaler of Numata et al. with a frequency prescaler which includes all the listed above limitation/details, as taught by Welty et al., that is suitable for fabrication in integrated circuit form in which the divide ratio thereof can be altered after fabrication would have been obvious to one of ordinary skill in the art at the time of the invention since Welty et al. teaches that such a configuration would satisfy the desire of altering the divide ratio without altering the number of flip-flop circuits used (*see Welty et al., col. 1, lines 56-58 and col. 2, lines 1-4*).

***Allowable Subject Matter***

9. Claims 12-16 and 26-29 are allowed.

Claims 3-5, 8-11, and 20-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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10. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art on record does not show or fairly suggest:

- A frequency prescaler including a third sequential element and the at least one logic gate is coupled to receive a signal from the output node of the first sequential element and is coupled to receive a signal from the third sequential element, as called for in claim 3;
- A frequency prescaler including a third sequential element having an output node coupled to an input node of the at least one logic gate of the first sequential element, and configured to decode a state of the asynchronous counter, as called for in claim 8;
- An even/odd modulus prescaler including a first true single phase clock flip-flop having an input stage with an embedded logic gate to decode a state of the asynchronous counter, configured to modify a modulus of the asynchronous counter between an even modulus and an odd modulus, in combination with the remaining claimed limitations, as called for in claim 12;
- A frequency synthesizer, in which the at least one true single phase clock flip-flop further includes a decoder flip-flop to decode a state of the least significant flip-flop and the more significant flip-flop, as called for in claim 20; and
- A method including decoding a state of the first and second sequential elements; and conditionally gating an input signal to the first sequential element using a logic gate embedded in an input stage of the true single phase clock flip-flop, as called for in claim 26.

***Citation of Relevant Prior Art***

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.



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Prior art Kim (U.S. Patent No. 6,411,669) discloses a dual-modulus prescaler for RF synthesizer.

Prior art Knapp (U.S. Patent No. 5,969,548) discloses a frequency divider with low power consumption.

***Inquiry***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Linh M. Nguyen  
Examiner  
Art Unit 2816

LMN

